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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,120	09/22/2003	Takashi Miyazawa	117244	5416

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/665,120	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,13,14 and 20-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13,14 and 20-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *27 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 21 May 2007. Claims 1-8, 13-14 and 20-33 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-8, 13-14 and 20-31 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-2, 4, 6-8, 13-14, 20-28 and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al. (US 2003/0098828) in view of Sempel et al. (US 2002/0027422).

Regarding claim 1, Hunter et al. discloses an electronic circuit (Figure 3), comprising:

a capacitor stores a current signal supplied to the capacitor and a voltage signal supplied to the capacitor (Figure 3, capacitor 24); and

a first transistor that includes a first gate, a first drain and a first source (Figure 3, transistor 22),

a conduction state of the first transistor being set in accordance with a charge stored by the capacitor (Figure 3 shows the gate of the transistor 22 connected to capacitor 24 and thus the conduction state will be controlled by the capacitor.), and

a first current as the current signal flowing through the first transistor when the capacitor stores the current signal (Paragraph [0037]).

Hunter et al. fails to teach no current flowing through the first transistor during the second period when the capacitor stores a voltage signal.

Sempel et al. disclose an electronic circuit (Figure 5) where a capacitor stores a current signal and where current flow through a first transistor, whose conduction state is controlled by a capacitor, is controlled by a switch (Figure 5 shows a transistor 21

whose gate is connected to capacitor 24. Figure 4 and paragraph [0021] explain that switch 11 controls whether transistor 21 allows current to flow or not.).

Thus, integrating the switch 11 taught by Sempel et al. into the circuit taught by Hunter et al. will create a circuit which can supply a voltage or a current signal, and where the current flowing through a first transistor can be controlled. Thus, the capacitor will store a current signal during a period when the current is to be supplied and the capacitor will store voltage when a voltage signal is supplied. The claim requires that the capacitor stores a current signal during a first period. The examiner understands that when the device is in current mode, the writing will be done as in Figure 4 of Sempel et al. The examiner then understands that the capacitor stores charge from a current signal during time t_F, which the examiner considers the first period. Thus when switch 11 is turned on at the end of the period as explained in paragraph [0037] of Sempel et al., current will flow through the transistor as required by the claim, i.e. current will flow during at least part of the first period. The examiner also understands that when the device is then switched into voltage mode, the writing will also be done as in Figure 4 of Sempel et al. The examiner then understands that the capacitor stores charge from a current signal during time t_{charge}, which the examiner considers the second period. Thus since switch 11 is turned off the entire period as explained in paragraph [0037] of Sempel et al., current will not flow through the transistor as required by the claim, i.e. no current will flow during the second period.

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to integrate switch 11 of Sempel et al. in the circuit taught by Hunter et al. in order to provide a more efficient lighting period.

Regarding claim 2, Hunter et al. and Sempel et al. disclose the electronic circuit according to Claim 1.

Hunter et al. disclose the circuit further comprising:

a second transistor (Figure 3, transistor 16),

the current signal and the voltage signal being supplied to the capacitor through the second transistor (Figure 3).

Regarding claim 4, Hunter et al. and Sempel et al. disclose the electronic circuit according to Claim 1.

Sempel et al. also disclose a fourth transistor that controls a timing to start or stop supply of the current to the electronic element after the conduction state of the first transistor is set according to at least one of the current signal and the voltage signal (Figure 5, switch 11, where it is well known to make a switch a transistor.).

Regarding claim 6, please refer to the rejection of claim 1, and furthermore Hunter et al. also disclose of a plurality of scanning lines (Figure 1, elements 4), a plurality of data lines (Figure 1, elements 6), a first circuit for outputting a current signal (Paragraphs [0011] and [0040]), a second circuit for outputting a voltage signal

(Paragraphs [0011] and [0040]), and a first electrode opposite a plurality of second electrodes, each included in one electro-optical elements (Figure 3 shows element 2 with a first and second electrode, where the second electrode of all the plurality of circuits is connected to ground.).

Regarding claim 7, Hunter et al. and Sempel et al. disclose the electro-optical device according to Claim 6.

Hunter et al. also disclose the current signal and voltage signal being supplied to each of the plurality of unit circuits through one data line of the plurality of data lines (Figure 3, data line 6.).

Regarding claim 8, Hunter et al. and Sempel et al. disclose the electro-optical device according to Claim 6.

Hunter et al. also disclose the plurality of data lines including a plurality of first data lines and a plurality of second data lines, the current signal being supplied to each of the plurality of unit circuits through one first data line of the plurality of first data lines; and the voltage signal being supplied to each of the plurality of unit circuits through one second data line of the plurality of second data lines (Figure 3 shows adjustment circuit 40 which provides two data lines, one for the current signal and one for the voltage signal.).

Regarding claim 13, Hunter et al. and Sempel et al. disclose the electro-optical device according to Claim 22.

Hunter et al. also disclose the electro-optical element being an EL element (Figure 3, element 2).

Regarding claim 14, Hunter et al. and Sempel et al. disclose the electro-optical device according to Claim 13.

Hunter et al. also disclose the EL element including a light-emitting layer that is composed of an organic material (Paragraph [0034]).

Regarding claim 20, Hunter et al. and Sempel et al. disclose an electronic apparatus, comprising: the electro-optical device according to Claim 6 (Figure 1 of Hunter et al.).

Regarding claim 21, Hunter et al. and Sempel et al. disclose the electronic circuit according to Claim 1.

Hunter et al. also disclose of the current signal being a multi-valued data current and the voltage signal being a binary data voltage (Paragraph [0011]).

Regarding claim 22, Hunter et al. and Sempel et al. disclose the electro-optical device according to Claim 6, each of the plurality of unit circuits including an electro-

optical element (Figure 1 shows that each unit circuit has an OLED. See paragraph [0034]).

Regarding claim 23, please refer to the rejection of claim 1, and furthermore Hunter et al. also disclose the first transistor supplying a current whose amount is determined in accordance with the conduction state to an electronic element (Paragraph [0037]).

Regarding claim 24, please refer to the rejection of claim 23, where the first mode is a current mode corresponding to the first period, and the second mode is a voltage mode that corresponds to the second period.

Regarding claim 25, this claim is rejected under the same rationale as claim 21.

Regarding claim 26, this claim is rejected under the same rationale as claim 21.

Regarding claim 27, Hunter et al. and Sempel et al. disclose the electronic circuit according to Claim 24.

Hunter et al. also disclose of power consumption in the second mode being lower than a power consumption in the first mode (Paragraph [0043]).

Regarding claim 28, this claim is rejected under the same rationale as claim 2.

Regarding claim 30, Hunter et al. and Sempel et al. disclose the electronic circuit according to claim 1.

Hunter et al. also disclose the electronic circuit further comprising:

an electronic element (Figure 3, element 2),

a second current whose current level corresponds to the conduction state of the first transistor being supplied to the electronic element (Paragraph [0037]).

Regarding claim 31, Hunter et al. and Sempel et al. disclose the electronic circuit according to claim 6, ca potential of the first electrode being set at a constant during at least a part of a first period in which the current signal is supplied to the capacitor, and the potential of the first electrode being set at the constant during at least a part of a second period in which the voltage signal is supplied to the capacitor (As explained in the rejection of claim 1, since no current will flow due to switch 11 of Sempel et al., the potential of the first electrode will be constant at least part of the first and second periods.).

Regarding claim 32, Hunter et al. and Sempel et al. disclose the electronic circuit according to claim 6.

Hunter et al. also disclose the current signal corresponding to analog data current, and the voltage signal corresponding to digital data voltage (Paragraph [0011]).

Regarding claim 33, Hunter et al. and Sempel et al. disclose the electro-optical device according to claim 6.

Hunter et al. also disclose the current signal corresponding to analog data current, and the voltage signal corresponding to digital data voltage (Paragraph [0011]).

6. Claims 3 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al. (US 2003/0098828) in view of Sempel et al. (US 2002/0027422) and further in view of Howard (US 2003/0052614).

Regarding claim 3, Hunter et al. and Sempel et al. discloses the electronic circuit according to Claim 1.

Hunter et al. and Sempel et al. fail to teach that the circuit comprises a third transistor that controls an electronic connection between the first gate and the first drain.

Howard discloses an electronic circuit comprising a third transistor (Figure 3A, Q4) that controls an electronic connection between a first gate and a first drain (As shown in Figure 3A the transistor Q4 has its drain connected to the gate of Q1 meaning that Q4 will control Q1's electrical connection.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to add the transistor taught by Howard into the circuit taught by the combination of Hunter et al. and Sempel et al. in order to provide more controlled current and voltage flow in the circuit.

Regarding claim 29, this claim is rejected under the same rationale as claim 3.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Howard (US 2003/0052614) in view of Dawson (US 6,229,506).

Regarding claim 5, Hunter et al. and Sempel et al. the electronic circuit according to Claim 1.

Hunter et al. and Sempel et al. fail to teach a fifth transistor, the amount of charge held in the capacitor being reset to a predetermined state when the fifth transistor is turned on.

Dawson discloses a transistor, the amount of charge held in a capacitor being reset to a predetermined state when the transistor is turned on (Figure 2, item 270; column 3, lines 20-22 and lines 44-52).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to include a reset transistor as taught by Dawson into the pixel circuit taught by the combination of Hunter et al. and Sempel et al. in order to reduce current nonuniformities and threshold voltage variations in a drive transistor.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

18 June 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER